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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,956	12/15/2003	Joel Hatsch	068758.0151	3388

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EXAMINER	
MAI, TAN V	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,956	HATSCH ET AL.	
	Examiner	Art Unit	
	Tan V Mai	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/5/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The abstract of the disclosure is objected to because legal phraseology is used in this paragraph (i.e., "comprises"). Correction is required. See MPEP § 608.01(b).

2. The drawings are objected to because Fig. 4 should be labeled "PRIOR ART". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Claims 2-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 2, the term "a and" (line 2) is NOT understood.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Niehaus et al.

As per independent claim 1, Niehaus et al teach, e.g., see Figs. 1 & 3-8, Abstract, Claim 1, col. 1, lines 8-12, and col. 6, lines 50-54, the claimed combination elements.

As per dependent claim 2, Figs. 3-8 show the claimed "each adder subblock is implemented from a maximum of three series-connected logic gate stages".

As per dependent claim 3, Figs. 3-5 and 8 show the detail of the claimed "first adder subbclock".

6. Claims 1-2 and 5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Song et al (Applicants' admission Prior Art, Reference #4).

As per independent claim 1, Song et al teach, e.g., see page 1189, first incomplete paragraph "... That is the reason why high-order **counters**, like **(7,3)** ... High-input counters can be designed directly by using folded transistors, as shown in **Fig. 6**, where we have **drawn the circuitry for output pairs** y_2 and y_2' of the (7,3) counter. **This concept can be extended to the other output pairs in a**

straightforward way". The discussion indicates the counter has at least 6 inputs & 3 outputs and three parallel subblocks as claimed.

As per dependent claim 2, Fig. 6 shows the claimed "each adder subblock is implemented from a maximum of three series-connected logic gate stages".

As per independent claim 5, Song et al do teach the added "each adder subblock consists of multitransistor circuit which cannot be resolved in to logic gates" feature, e.g., see "... That is the reason why high-order counters, like (7,3) ... **High-input counters can be designed directly by using folded transistors, as shown in Fig. 6**, where we have drawn the circuitry for output pairs y_2 and y_2' of the (7,3) counter. This concept can be extended to the other output pairs in a straightforward way".

7. Claims 1-2 and 5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wang et al (Applicants' admission Prior Art, Reference #5).

As per independent claim 1, Wang et al teach, e.g., see pages 403-407 and Fig. 3, the claimed combination elements. It is noted that Wang et discuss "[t]his is sometimes referred to as a **5-3 compressor**, and is conventionally used in binary arithmetic circuits" (page 404, left col. last sentence) and "[w]e ..., that the designs resulting from the switching tree graph theoretic minimization procedure have acceptable charge sharing problem up to **6 inputs** for these types of adder/counter circuits". The discussion, equation (1) and Fig. 3 indicate the circuit has 6 inputs & 3 outputs and three parallel subblocks as claimed.

As per dependent claim 2, Figs. 1 & 3 show the claimed "each adder subblock is implemented from a maximum of three series-connected logic gate stages".

As per independent claim 5, Wang et al do teach the added "each adder subblock consists of multitransistor circuit which cannot be resolved in to logic gates" feature, e.g., see Fig. 3.

8. Claims 1-2, 5 and 8 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Dhong et al (Applicants' admission Prior Art, Reference #3).

As per independent claim 1, Dhong et al teach, e.g., Figs. 1-4, the claimed combination elements.

As per dependent claim 2, Figs. 2-4 show the claimed "each adder subblock is implemented from a maximum of three series-connected logic gate stages".

As per independent claim 5, Wang et al do teach the added "each adder subblock consists of multitransistor circuit which cannot be resolved in to logic gates" feature, e.g., see Figs. 2-4.

As per dependent claim 8, the claim adds the "charging circuit" feature. Dhong et al's circuit is a dynamic device.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Niehaus et al.

Niehaus et al have been discussed in paragraph #5 above.

As per dependent claim 4, the claim adds the "NAND" gates feature in all three stages. The detail feature is obvious to a logic designer in the art because "NAND" or "NOR" gates are simple logic gates. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Niehaus et al's teachings because the device is 6 to 3 binary adder as claimed.

11. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al.

Song et al have been discussed in paragraph #6 above.

As per dependent claims 6-7, the claims add the detail interconnection in transistor level of the adder subblocks for calculating the carry bit of weight 2w & 4w. Song et al's Fig. 6 shows the detail interconnection in transistor level. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Song et al's teachings because the counter (7,3) includes 6 to 3 binary adder as claimed.

As per dependent claim 8, the claim adds the "charging circuit" feature. The feature is old and well known in the "dynamic circuit technology".

12. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al.

Wang et al have been discussed in paragraph #7 above.

As per dependent claims 6-7, the claims add the detail interconnection in transistor level of the adder subblocks for calculating the carry bit of weight 2w & 4w. Wang et al's Fig. 3 shows the detail interconnection in transistor level. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Wang et al's teachings because the circuit includes 6 to 3 binary adder as claimed.

As per dependent claim 8, the claim adds the "charging circuit" feature. The feature is old and well known in the "dynamic circuit technology", e.g., Fig. 1 has clock feature.

13. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhong et al.

Wang et al have been discussed in paragraph #8 above.

As per dependent claims 6-7, the claims add the detail interconnection in transistor level of the adder subblocks for calculating the carry bit of weight 2w & 4w. Dhong et al's Fig. 2-4 show the detail interconnection in transistor level. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to design the claimed invention according to Dhong7 et al's teachings because the circuit includes 6 to 3 binary adder as claimed.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cited references are art of interest.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan V. Mai whose telephone number is (571) 272-3726. The examiner can normally be reached on Mon-Wed and Fri. from 9:30am to 2:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki, can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is:

Official (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Tan V. Mai
Primary Examiner